

# WHITE PAPER

5G Next Generation Core Network  
Intel® Programmable Acceleration Card  
with Intel® FPGA



# Enabling Communications Service Providers to Meet 5G High Density I/O Goals through Software Optimization and Hardware Acceleration

**Affirmed Networks' 5GCN cloud-native network function reached 200 Gbps on 100 GbE links using Intel® Xeon® Scalable processors and Intel® FPGA-based Programmable Acceleration Card and Dell EMC's PowerEdge\* server<sup>1</sup>**

Enabling cost-effective and scalable user plane 5G core solutions in cloud-native environments to serve both edge and central office requirements by utilizing an open source ecosystem and best-in-class compute platforms.

## Introduction

5G technology promises to greatly enhance the speed, coverage, and responsiveness of wireless networks and will drive new use cases such as interactive television, high-definition and 3D video, social gaming, virtual and augmented reality (VR and AR), robotics, automated vehicles, advanced manufacturing, and healthcare imaging. Some of these use cases require high bandwidth, while others require low latency. A new type of platform is needed to deliver the best of IT while meeting mobility network requirements. This new infrastructure will need to be cost-effective, flexible, easy to deploy and scale efficiently with growing traffic and services. These conditions can be met through an optimized, joint hardware and software solution using the leading COTS x86-based platforms and hardware acceleration by FPGA.

Intel, Affirmed Networks, and Dell EMC have developed a proof of concept for high-performance Next-Generation Core Networks (NGCN). This white paper presents a state-of-the-art solution for the commercial, standalone 5G core network (5GCN) that demonstrates the 100 Gbps/CPU socket (200 Gbps in the next-gen solution<sup>1</sup>) using a 100 GbE NIC interface and Intel® Xeon® Scalable processor-based server. The combination of software optimization and hardware acceleration resulted in the phenomenal 20 Gbps/pCore.

Smart load balancing using Intel® FPGA and CPU cache optimizations with Affirmed Networks' revolutionary 5G User Plane Function (UPF) enhances software performance of 5GCN applications. Intel FPGA acceleration addresses traditional I/O limitations, allowing termination of 100 GbE interfaces per CPU socket, 20 Gbps per core, and enabling 16 or more worker cores for packet processing.

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## Accelerated 5G Core Network Solution

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[Intel® Silicon Photonics](#)

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[Affirmed Networks 5G Core UPF cloud-native software solution](#)

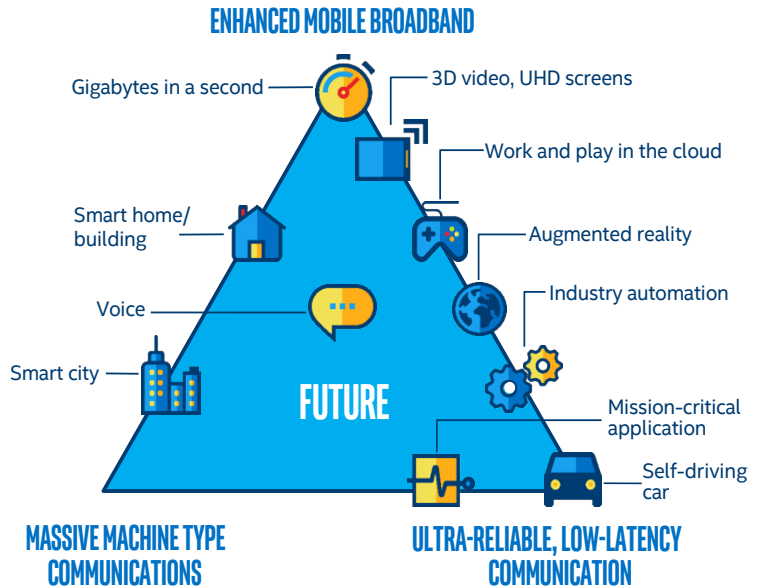
## 5G infrastructure

5G offers a new set of opportunities and challenges for mobile operators. The diversity of potential use cases drives a variety of requirements from the core network.

The growing services driven by 5G, edge computing, and IoT require mobile operators to build a new infrastructure—one that is highly available and can scale efficiently to accommodate a massive number of connected devices with the exponential rise of data traffic and different quality of service levels generated by different use cases. Current solutions that use specialized appliances will not be sufficient to support future 5G needs. Proprietary hardware is not only expensive but also not flexible enough to respond to evolving customer needs, as well as leverage an available developer ecosystem.

NFV has emerged as a means of providing the necessary resource flexibility to ensure high utilization and high levels of programmability to cover diverse workload profiles. NFV is built on best-in-class x86 infrastructure to provide optimal and cost-effective deployment. To further increase performance while preserving the form factor for these virtualized systems, Intel FPGAs deployed as COTS accelerator hardware can be utilized as an additional programmable element to provide energy and cost savings.

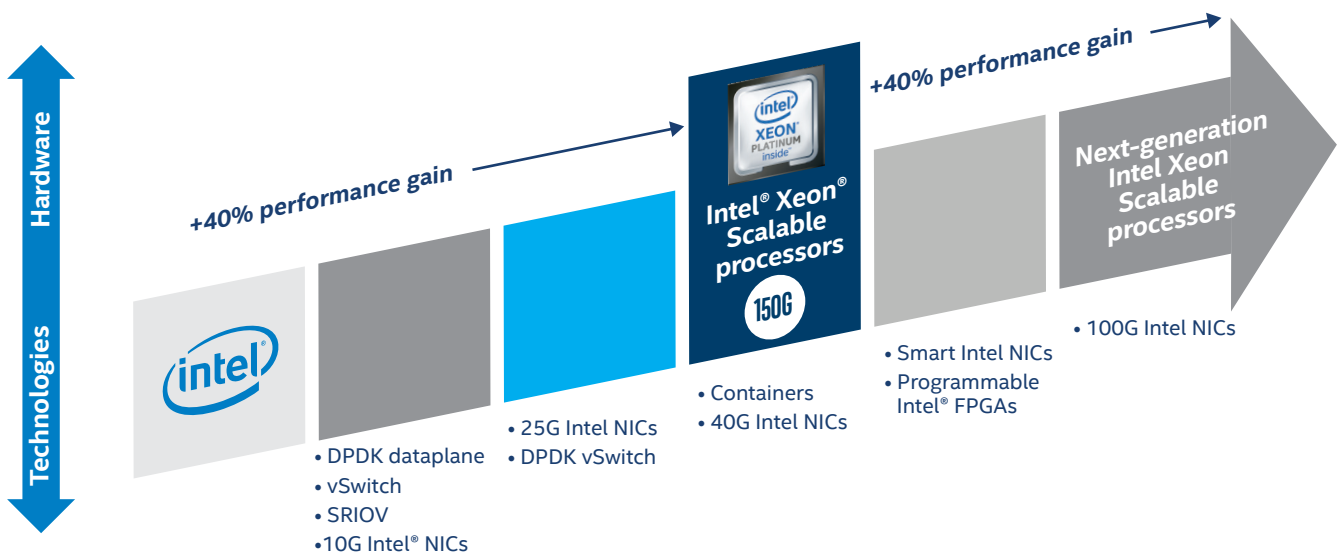
FPGA-accelerated solutions result in lower power consumption per bit and reduced latency compared to traditional solutions. They also allow the data rates to reach 400 Gbps on a single server using multiple cards or a multi-host approach (e.g., separate PCI\* per socket from a single card) and present fine-grained and diverse quality of service (QoS) characteristics across multiple network slices in 5G network deployment. Benefits of using the Intel® FPGA-based Programmable Acceleration Card (PAC) as a



5G network usage scenarios

hardware accelerator for communications networks include efficient scaling, increased throughput capacity, fast time to market, flexibility, and lower TCO. Intel® PAC supports data center best practices due to integration of Intel FPGA image management into NFV life cycles and scheduling of workloads benefitting from FPGAs into OpenStack\* services like Nova, Cyborg, and Neutron.

As demand shifts and changes over time, Intel FPGAs can be reprogrammed to optimally address the new requirements. Intel FPGAs have been used for many decades to accelerate a wide range of networking, compute, and storage workloads making them a versatile, common, new programmable component for carrier clouds.



### Intel, Dell EMC, and Affirmed Networks are delivering high performance and low cost per bit?

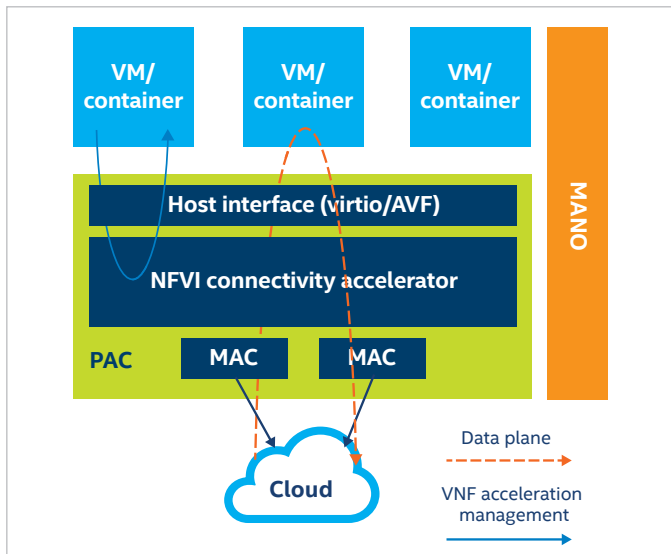
This new infrastructure will help lower CapEx and OpEx for new applications that demand high packet rates, maintaining line rate speeds for H-QoS, traffic shaping, virtual private networks (VPNs), firewalls, encapsulation, deep packet inspection, encapsulation/decapsulation, and myriad other applications that would have been cost prohibitive otherwise. Other NFV applications that benefit from such infrastructure include virtual broadband networking gateway (vBNG), virtualized core network (vEPC/5GCN), internet protocol security (IPSec), and beyond.

## Network functions virtualization (NFV) acceleration

Increasing overall server performance for VNFs in cloud environments is accomplished by leveraging a combination of aggressive software optimization in the user plane, acceleration of NFVI and selected VNFs' functionalities, and additional data center architectural enhancements. Efficient packet processing requires tools, such as the Data Plane Development Kit (DPDK) and Vector Packet Processing (VPP), to reduce related bottlenecks and CPU cache contention. They present a new approach where using Poll Mode Drivers (PMD) and software techniques make it possible to keep the network data inside the CPU cache as long as possible, which increases overall system performance.

The VNF can be hosted within either a VM or a container. A single FPGA can be shared between multiple VNFs. The FPGA connects VNFs with a cloud network and acts as an accelerator for VNF-level and network infrastructure. The FPGA resource is controlled by an orchestrator from resource discovery to allocation. Some examples of acceleration are H-QOS in vBNG under VNF and OVS and vRouter under NFVI acceleration. In this PoC, accelerated load balancing across VNF cores provided additional performance.

In accelerated 5GNC, VNF acceleration with the host interface is used to achieve high throughput, enabling the 100 Gbps/socket solution and reaching to 20 Gbps/pCore. Performance enhancement is achieved through CPU cache optimization and core-level load balancing. The software-based 5GCN solution can only work effectively when packets are properly distributed between CPU cores. It is efficient to use the same CPU core for a specific session on both uplink and downlink directions, since a large amount of information in both directions is shared (e.g., DPI and some counters). This type of load balancing is very difficult and complex, as different fields of the packet are used for decision-making depending on the packet direction. The load balancing challenge can be addressed in different ways (e.g., DDP, FPGA acceleration). This white paper focuses on use of FPGA as a load balancing accelerator. All 5GCN traffic comes to the PAC and the PAC is aware of the traffic direction and can use any set of packet fields to spread traffic received by the application to many hardware queues.



NFVI and VNF acceleration with the Intel® PAC

Orchestration frameworks such as OpenStack can allow users to consume FPGAs the same way as any hardware resources in NFVI. The orchestrator discovers the hardware accelerator resources. For example, the Intel PAC allocates and reprograms based on VNF requests and at the end of the life cycle terminates the allocation and releases the resource.

### Benefits of using Intel FPGAs as NFV accelerators

Intel PAC for NFV offers the hardware and IP flexibility to support today's popular workloads and can be programmed to support future workloads.

- Improve bandwidth to meet ever-growing demand
- Enhance performance
- Programming and reprogramming capability to adapt to different acceleration solution needs
- Scale to diverse and evolving applications
- Augment the system with a flexible acceleration solution, increasing total system capabilities
- Offer a more deterministic solution for total system performance and latency
- Gain the flexibility for evolving standards
- Leverage acceleration of selected workloads to free up system resources for additional workloads
- Achieve total cost of ownership (TCO) goals
- Fast time to market
- Support OpenStack orchestration
- Leverage developer tools and libraries
  - Data Plane Developer Kit (DPDK)
  - Open Programmable Acceleration Engine (OPAE)
  - Intel Quartus® Prime Software and the Intel® FPGA SDK for OpenCL™ Application Developers

### Benefits of Affirmed Networks EPC/5GNC software optimization

- Complements hardware optimization
- Designed to leverage forthcoming PCIe\* Gen 4 2x speedup in servers
- Use of SR-IOV, DPDK, and VPP to further improve core efficiency
- Supports advanced features such as DPI, CG-NAT, TCP optimization, and QUIC video rate adaptation
- Supports individual elephant sessions (e.g., 20 Gbps downlink, 10 Gbps uplink)
- Allows selection of smaller servers and/or mixing of general workloads with I/O-heavy workloads
- Scales from very small for applications at the far edge to very large for traditional, centralized core deployments

## Challenges of 5G core networks

Control and User Plane Separation (CUPS) enables separation of control and user plane functionality in the core network. This allows flexible network deployment and operation, as well as independent scaling between control plane and user plane functions. Consequently, data forwarding can be decentralized with packet processing and traffic aggregation closer to the edge. Potential benefits include improved session management, end-to-end network slicing, seamless mobility, and support for cloud native applications.

The User Plane Function (UPF) is a component of a 3GPP 5G architecture facilitating operation of the user plane and was integrated by 3GPP as a critical part of 5GCN. (Learn more about 3GPP at [3gpp.org](http://3gpp.org).)

Edge breakout for location-sensitive, location-based, and low-latency services presents an exciting opportunity for 5GCN. A far greater quantity of UPF deployments will result, further highlighting the advantages of a cloud native approach. These include improved dynamic range of deployments from very small to very large; ease of deployment and life cycle management through container orchestration engines such as Kubernetes\* and Helm\*; superior observability; and the ability to aggregate logs, traces, and KPIs from edge deployments to regional aggregation data centers.

5G networks can improve the user experience through network slicing in enterprise-level networks. Network slicing is a powerful tool that introduces flexibility over a shared physical communication channel by creating multiple logical slices over the physical channel. Network slicing will help meet the cost, efficiency, and flexibility requirements imposed by 5G and users' demands. Network slicing is a big driver for moving network services from an appliance model to the more flexible, easier-to-maintain data center model familiar from cloud—where services can be implemented as software applications running on COTS servers. Unfortunately, moving core network services to the data center creates some new challenges that were not present in the appliance model.

One of the challenges related to LTE EPC management is the assignment of a user equipment (UE) to one specific LTE EPC server line. According to the LTE specification, only one line card has knowledge about traffic generated by a user, the subscription, QoS requirements, counters, and statistics. There is no distributed engine that can handle traffic from a single user device attached to the mobile core and only one specific LTE EPC line card can perform functions. For example, user session management is performed on the user level, not on the specific session level. Fulfilling this requirement is not a problem in a traditional appliance model, where the base station handling traffic from a user device is simply connected to the LTE EPC line card by some equivalent of the wire. The 5GNC specifications accept the LTE management for compatibility reasons. They also propose different methods of UE assignment that can make handling these issues easier.

The data center model of network traffic handling is very different from traditional LTE EPC models. In the data center, every user session can be handled by different servers in different locations. Every HTTP connection from the same user can be handled by different servers. This model has proven to be very effective and scalable. Inside the data center, there are many devices called load balancers trying to distribute traffic from a single user as much as possible across data center resources, using hash-based algorithms.

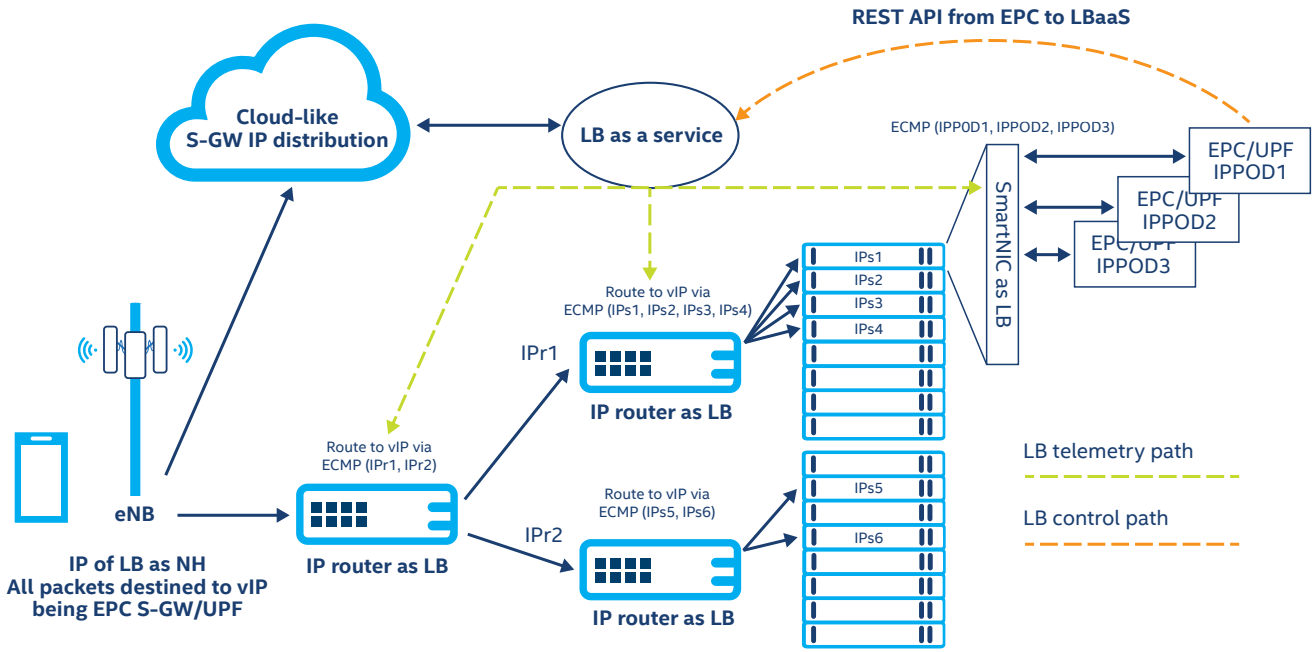
With the advent of 5G cloud-generation mobility infrastructure implemented in the data center, there is a seemingly contradictory requirement on how to meet the 5GCN/EPC specifications to handle all traffic from a single device using a single line card represented by a single server application, where traffic that should be received by one server is distributed over multiple servers.

A common practice used by many vendors is that the 5GCN/EPC service (being a software application) is used to implement special engines that create a virtual mesh of line cards inside their applications. For a given user session, traffic should be handled by a specific line card. If it was received by that specific line card, it has to resend to that specified line card. This traffic approach is very expensive, as a large amount of east west traffic can be generated. Simple probability proves that when a system contains 100 line cards in the network, only 1 percent of the traffic from users will be received on the proper line card.

This problem can be solved in multiple ways. Depending on the deployed 5GCN solution, operators can use specialized 5GCN load balancers, but no other applications will be able to use it. Another possibility is to use ECMP in standard routers to distribute the traffic, but this needs to be managed intelligently. Operators can also limit the number of servers playing the role of line cards by implementing the groups of servers managed by Load Balancer as a Service (LBaaS) features.

In the data center, one line card is normally represented by a single application that cannot share the NICs' interfaces. Even using a single server and multiple line card applications does not solve the traffic distribution problems properly since, logically, these applications behave as separate line cards that cannot exchange their data, yet still need to exchange east west traffic. Compared to using data center network infrastructure, distribution can be done more effectively on server-level traffic, but this still causes many issues. This is a primary reason why 5GCN vendors seek to handle more and more traffic using a single server application.

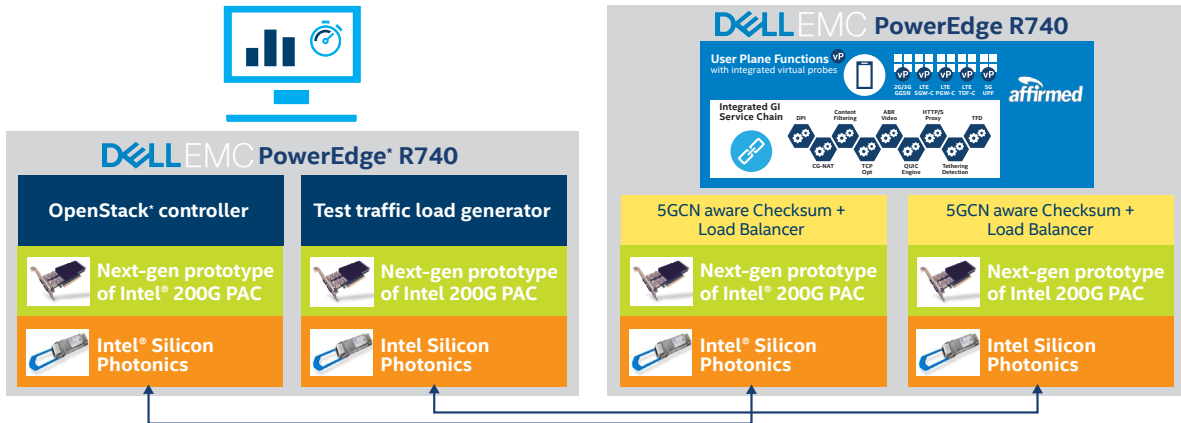
The demand to limit the number of line cards generates a need to move from multiple 25 GbE cards to 100 GbE cards and faster interfaces per server. A faster interface connected to a traffic load balancer decreases the probability of generating east west traffic between servers (i.e., what makes the 5GCN/EPC system more effective).



5GCN/EPC load balancing

### Solution overview

Intel, Dell EMC, and Affirmed Networks present a solution for 5GCN/EPC that pushes boundaries and presents the true 100 Gbps/CPU socket solution using a single Intel® Network Interface Card (Intel® NIC) interface running on a Dell EMC PowerEdge® R740 server powered by Intel Xeon Scalable processors and realized in a 5G data plane UPF from Affirmed Networks. This is the first cloud native solution supporting 100 GbE interfaces.



The first virtualized 5GCN solution supporting 100 GbE interfaces

The traditional software and hardware approach for VNF applications uses a single SRIOV Virtual Function (VF) device per VNF. This limits the performance of the VNF by the number of the NIC queue assignment per application worker (the typical amount the XL710 VF feeds is 16 CPU cores). Using the Intel FPGA for smart load balancing and CPU cache optimizations enhances software performance and makes it possible to realize the SR-IOV VF-bonding feature which breaks through traditional I/O limitations, allowing termination of 100 GbE interfaces per CPU socket and enabling more than 16 worker cores for packet processing per 5GCN/EPC application.

The result is the first Next-Generation Core Network (NGCN) 100 Gbps socket solution (200 Gbps for 2-socket server!), improved software efficiency and cache optimization via the

Intel® Stratix® FPGA accelerator, lower power consumption per bit rate, and reduced latency compared to traditional solutions. These optimizations enable a 200 GbE solution with a path toward 400 GbE.<sup>1</sup> Specifically, as next-generation servers with PCIe Gen 4x16 slots become available, 200 Gbps<sup>1</sup> per socket can be terminated, given that the current solution uses less than 50 percent<sup>3</sup> of the vCPUs. The combined benefits make it possible to present fine-grained and diverse QoS characteristics across multiple network slices in 5G network deployments. Slice categories include enhanced Mobile Broadband (eMBB), massive IoT (mIoT), and Ultra-Reliable Low-Latency Communications (URLLC), with any number of slice instances in each category to support single tenancy isolation when desired.

This 5GCN solution incorporates Affirmed Networks' ground-breaking cloud native 5GC software running in an open source Data Plane Development Kit (DPDK) ecosystem, accelerated by the Intel PAC running on high-performance, Intel Xeon Scalable processor-based Dell EMC PowerEdge servers.

- **Affirmed Networks 5G Mobile Core\***, built on a web-scale architecture, enables rapid delivery of new services and the unlimited scale that operators require to provide outstanding service levels, self-service functionality, and faster activation times.
- **Dell EMC PowerEdge R740 Servers** powered by Intel Xeon Scalable processors, offering enhanced compute, network, and storage capabilities with flexible resources to address diverse workloads.
- **Next-generation prototype of Intel FPGA-based PAC for networking**, a custom-defined, programmable acceleration card for NFV application acceleration fully integrated as a manageable accelerator device supported by OpenStack with Nova, Cyborg, and Neutron supporting a standard VNF life cycle.
- **Intel® Silicon Photonics** to help meet 5G fronthaul network requirements with significant performance, cost, and scale benefits.

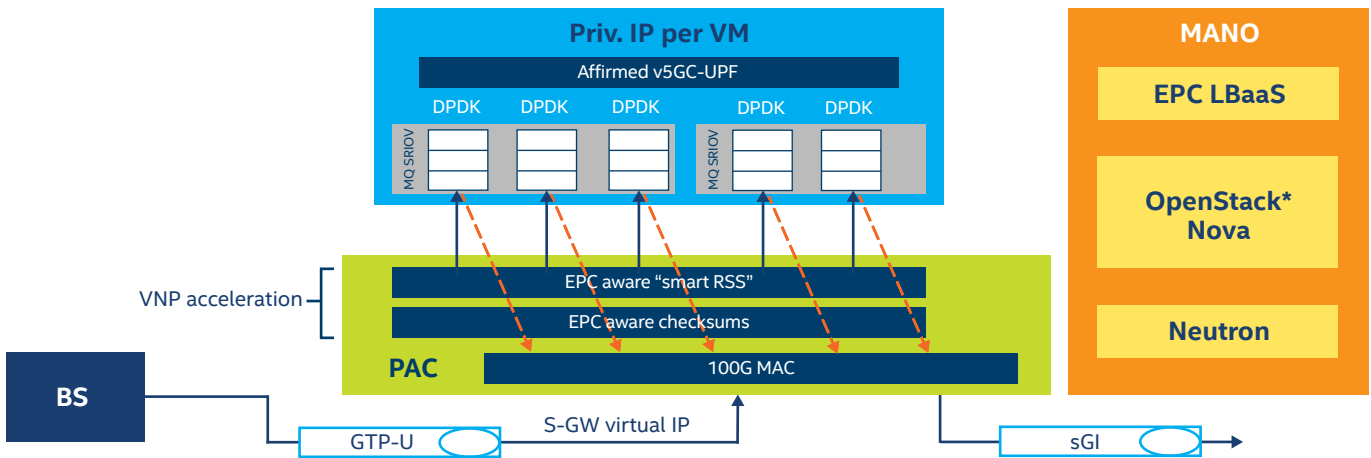
### Load balancing acceleration based on Intel FPGA

The 5GCN application is based on the Data Plane Development Kit (DPDK) and uses multiple CPU cores to handle traffic so the application design on the server level should limit synchronization issues between cores used for packet processing.

The 5GCN software can be designed as a single worker or multi-worker. The sample solution is managed by OpenStack and contains a 5GCN application from Affirmed Networks, as well as the traffic generators.

More server traffic requires the UPF to work more effectively. Traditional ASIC technology can only achieve 100 GbE performance per server CPU socket using multiple cards, where every card has a separate MAC address and appears as a separate NIC. This still creates problems with east west traffic generation. The solution for this issue is to emulate a true 100 GbE interface that directly connects to another 100 Gbps router/switch device.

From the software perspective, a packet load balancer based on analyzing and distributing traffic across the worker cores is very compute resource hungry. This functionality has been removed and replaced with a hardware load-balancer using an Intel PAC.



### Intel® PAC distributes workloads across the applications running on the server

The PAC embeds two Intel® Ethernet Controller XL710 NICs and a bump-in-the-wire Intel FPGA on board with two real 100 GbE interfaces. Achieving 100 GbE in that model requires first implementing load distribution using the Intel FPGA to distribute traffic fairly between two 50 GbE Intel® Ethernet Controller XL710 ASICs. For the 5GCN/EPC application, these Intel Ethernet Controller XL710 ASIC interfaces appear as a “super” device able to provide more queues than a single VF interface. This is called a load distributor driver.

The Intel PAC with load-balancing functionality fairly distributes traffic by using a smart RSS algorithm on the micro-flow level. The 5GCN/EPC-aware smart RSS makes it possible to steer traffic to put traffic from a specific 5GC session on the same CPU core, regardless of which direction traffic goes through the 5GCN/EPC (uplink or downlink). The smart RSS makes it possible to optimize CPU cache usage

in the optimal way by avoiding traversing traffic to and from user equipment using different cores. Once load balancing happens in the Intel PAC—at 100 Gbps per socket—network optimization continues, with software running on Intel Xeon Scalable processor-based Dell EMC PowerEdge Servers to handle functions including the remaining charging, egress and ingress for QoS, and scheduling cores.

The Affirmed 5G Cloud Native UPF was able to drive maximum possible line rates on the 200 G prototype Intel PAC. The effective payload (no protocol overhead) throughput achieved was close to 170 Gbps with only 12 pCores. In scale down mode with 8 pCores, each pCore achieved 20 Gbps. Through hardware load balancing, 12 cores were freed, creating a lot of headroom on the Intel® Core™ processor-based server for functions such as DPI, vProbe\* record streaming, and QUIC\* video rate adaptation. The reduction in the effective throughput

was primarily because of known overhead caused by IP packet headers and acceleration metadata. However, due to the nature of the 5GCN application, the links can never be saturated if all the links process a mix of GTP-U traffic and non-GTP-U traffic.

By utilizing the smart RSS to offload the micro flow-level traffic and distribution among the UPF cores, the solution ensures a right balance by keeping flow learning and other complex stateful packet inspection and processing in the UPF application. This is suited for mobility and 5G workloads, instead of completely offloading packet processing to the FPGAs.

WHAT COMMUNICATIONS SERVICE PROVIDERS WANT	WHAT THE INTEL®, DELL EMC*, AND AFFIRMED NETWORKS* SOLUTION DELIVERS
<p><b>High-density I/O</b></p> <ul style="list-style-type: none"> <li>• High performance and cost-effective (core/watt/square foot)</li> </ul> <p><b>Cloud native solution</b></p> <ul style="list-style-type: none"> <li>• Scalable</li> <li>• Stateless</li> <li>• Highly available</li> <li>• Simple in-service upgrade</li> </ul>	<p><b>Smart selection of accelerated workloads from both CNF and NFVI to FPGA</b></p> <ul style="list-style-type: none"> <li>• Acceleration of 5GCN load balancing</li> </ul> <p><b>Performance enhancement</b></p> <ul style="list-style-type: none"> <li>• CPU cache optimization</li> <li>• Core load distribution</li> </ul> <p><b>CPU bottleneck removal for 200+ Gbps<sup>1</sup></b></p> <ul style="list-style-type: none"> <li>• Cloud-friendly solution</li> <li>• Scalable networking with 100 GbE support and agile software life-cycle management</li> <li>• Use with any public or private cloud</li> </ul>

### Quick glossary

**5GCN:** 5G Core Network

**CNF:** Cloud Native Function

**COSP:** Communication Service Provider

**COTS:** Commercial Off-the-Shelf

**EPC:** Evolved Packet Core

**H-QoS:** Hierarchical Quality of Service

**IPSec:** Internet Protocol Security

**OVS:** Open vSwitch

**NFV:** Network Functions Virtualization

**NGCN:** Next Generation Core Network

**QoS:** Quality of Service

**vBNG:** Virtual Broadband Network Gateway

**vEPC:** Virtualized Evolved Packet Core

**VNF:** Virtual Network Functions

## Solution components

### Next-generation prototype for Intel PAC for networking

This custom-defined Intel FPGA-based programmable acceleration card provides NFV acceleration.

INTEL® STRATIX® 10 FPGA-BASED PAC	
<b>Acceleration functions</b>	<ul style="list-style-type: none"> <li>• Includes example IPs from Intel for VNF (BNG, EPC) and NFVI (vRouter) acceleration functions</li> <li>• Leverages existing IP from Intel and third parties</li> <li>• Optimized for ~60 150W TDP</li> </ul>
<b>Capacity</b>	<ul style="list-style-type: none"> <li>• 2x100 GbE network interfaces</li> <li>• 2xPCIe3x8 when the XL710 chip is used or 1xPCIe Gen3 x16</li> <li>• 9GB DDR4, 144 Mb QDR4 memory</li> </ul>
<b>Dual Intel® Ethernet Controller XL710</b>	<ul style="list-style-type: none"> <li>• Extensive OS support</li> <li>• Simplified system integration</li> <li>• Dual 40 Gbps pipeline</li> </ul>

The solution described in this paper is based on the next-generation prototype PAC, but it will also be available on productized PACs, such as Intel® FPGA PAC N3000.

## Intel® FPGA Programmable Acceleration Card N3000 for Networking (Intel® FPGA PAC N3000)

Intel's first 100 GbE programmable acceleration card designed for networking application acceleration.

Intel FPGA PAC N3000 is a highly customizable platform which enables high throughput, lower latency, and high-bandwidth applications. It allows for optimization of data plane performance to achieve lower costs while maintaining a high degree of flexibility. Support of end-to-end industry standard and open source tools streamline adaptation to evolve workloads and standards.

INTEL® FPGA PAC N3000	
<b>Targeted workloads</b>	<ul style="list-style-type: none"> <li>vBNG</li> <li>5GCN/vEPC</li> <li>IPSec</li> <li>SRv6 VPP</li> </ul>
<b>Key components and interfaces</b>	<ul style="list-style-type: none"> <li>Intel® FPGA PAC N3000 for Networking</li> <li>Intel® Arria® 10 FPGA</li> <li>9GB DDR4 + 144Mb QDR4</li> <li>8x10 GbE, 4x25 GbE</li> <li>PCIe® Gen3 x16 interface</li> <li>Supports Intel® Ethernet Controller XL710                             <ul style="list-style-type: none"> <li>-Extensive OS support and easier system integration</li> <li>-Dual 40 Gbps pipeline</li> </ul> </li> </ul>
<b>Board management</b>	<ul style="list-style-type: none"> <li>Intel® MAX® 10 FPGA Baseboard Management Controller (BMC)                             <ul style="list-style-type: none"> <li>-Temperature and voltage readout</li> <li>-Platform Level Data Model (PLDM)</li> <li>-Intelligent Platform Management Interface (IPMI 2.0)</li> </ul> </li> <li>Remote update of FPGA flash and BMC</li> </ul>
<b>Power and thermals</b>	<ul style="list-style-type: none"> <li>Intel® Enpirion® digital PowerSoC modules</li> </ul>
<b>FPGA interface manager</b>	<ul style="list-style-type: none"> <li>Common developer interface for Intel FPGAs</li> <li>Dynamically reconfigure the FPGA to suit the application workload acceleration demands</li> </ul>
<b>Developer tools and libraries for acceleration functions</b>	<ul style="list-style-type: none"> <li>Data Plane Developer Kit (DPDK)</li> <li>Open Programmable Acceleration Engine (OPAE)</li> <li>Intel Quartus® Prime Software and the Intel® FPGA SDK for OpenCL™ Application Developers</li> <li>Includes sample IPs from Intel for vBNG acceleration functions:                             <ul style="list-style-type: none"> <li>-H-QoS, classification, policing, scheduling, shaping</li> </ul> </li> </ul>

## Intel® Silicon Photonics

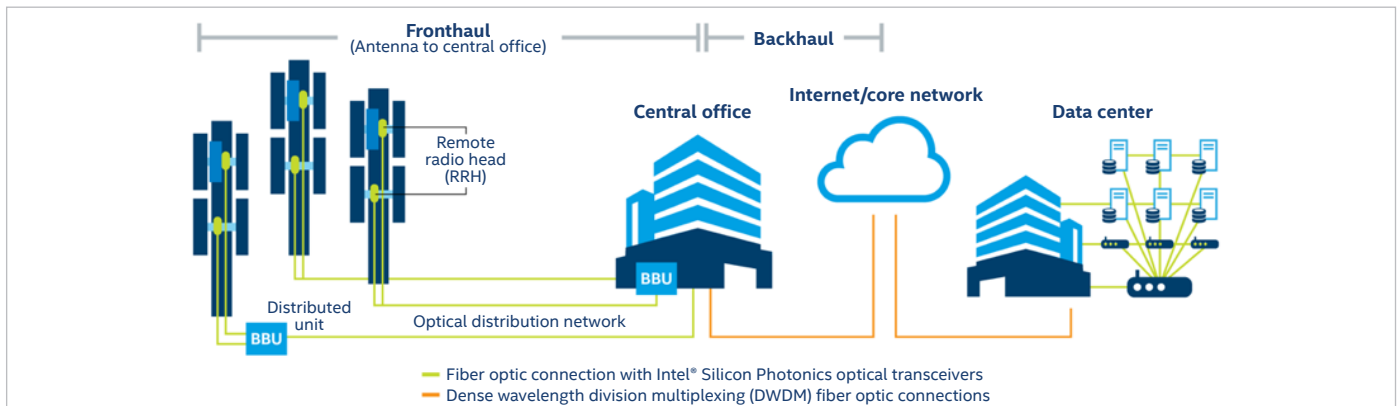
In many cases, networks are becoming less centralized and more complex, placing increased demands on the fronthaul network (the connection from the cell-site antenna to the central office where the baseband unit is housed), Intel Silicon Photonics can help meet 5G front haul network requirements.

Intel Silicon Photonics employs a hybrid laser approach, where the light-emitting capability is integrated with silicon at the wafer level. This approach removes the need for optical alignment and results in a manufacturing process that leverages Intel's high-volume silicon production capabilities, with significant performance, cost, and scale benefits.

Intel Silicon Photonics optical transceivers provide:

- High bandwidth, with transmission rates up to 100 Gbps
- An extended temperature range -40° to 85° C (as opposed to 0° to 70° C for standard commercial-grade transceivers) for extreme outdoor deployments
- Long transmission distances (up to 10 km)

As such, they are well suited to meet the needs of 5G fronthaul data transport requirements.





### Dell EMC PowerEdge R740 Servers

Dell EMC PowerEdge R740 servers are the bedrock of the modern data center. Powered by Intel Xeon Scalable processors, they enable both traditional and emerging workloads with up to 5x network throughput,<sup>3</sup> simple unified management, and multigenerational investment protection.

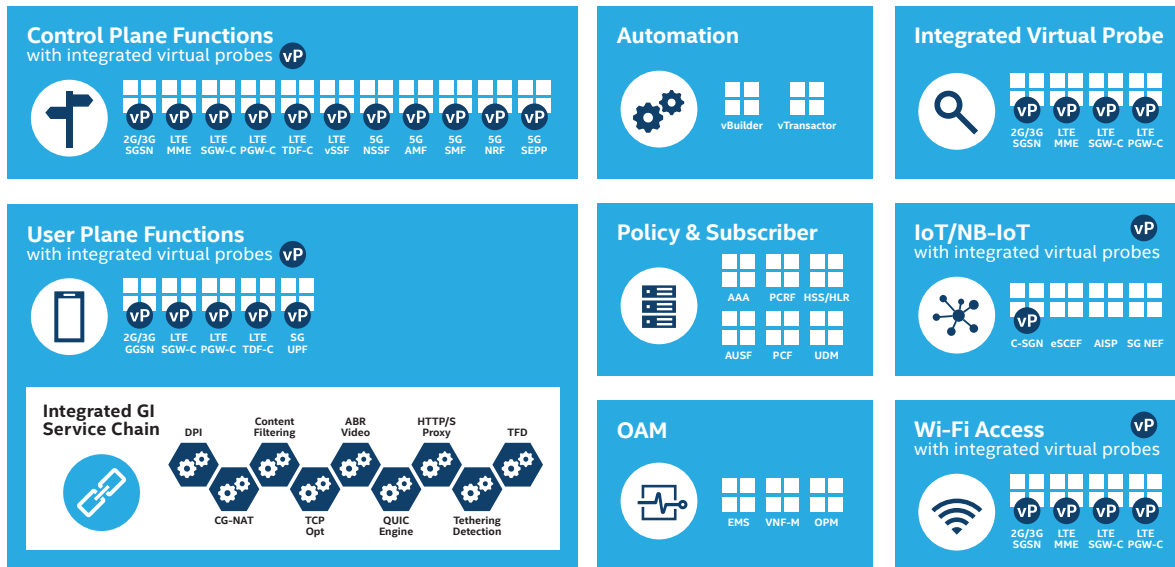
PowerEdge R740 servers offer scalable compute, network, and storage capabilities to address a wide range of workloads, so communications service providers can adapt quickly and address evolving business needs.

The servers enable a pervasive edge-to-core-to-cloud workload execution environment, supporting 5G workload automation at scale across administrative domains, multicloud, and cloud management platforms. Capabilities include differentiated workload profile execution; content caching and acceleration; and intelligent, data-centric policy decision and enforcement to help communications service providers deliver premium media-rich experiences.

- **Scalable business architecture:** Maximize performance across the widest range of applications with highly scalable architectures and flexible internal storage.
- **Intelligent automation:** Automate the entire server life cycle from deployment to retirement with embedded intelligence that dramatically increases your productivity.
- **Integrated security:** Protect your customers and your business with a deep layer of defense built into the hardware and firmware of every server.
- **Robust, mission-critical platform:** Designed for high-value and industrial-grade applications.
- **Support evolving workloads:** Handle workload diversity with intelligent grooming and acceleration, plus security and visibility.
- **Speed innovation:** Accelerate rollouts and mobile innovation time to market.
- **Increase flexibility:** Enable agile service portfolios.

### Affirmed Networks 5GC, 5G EPC VNF solutions

Affirmed Networks delivers a fully virtualized 5G webscale mobile core solution that supports both 5G EPC and 5GC. Built on microservices architecture, Affirmed Networks' solution capabilities include 5G NR, CUPS; network slicing (virtual slice selection function); optimized IoT access (NB-IoT/LTE-M/SCEF); virtualized Wi-Fi gateway (ePDG and TWAG); integrated virtual probe; virtualized DPI, GiLAN, analytics and security services; and the Affirmed Service Automation Platform\* (ASAP\*).



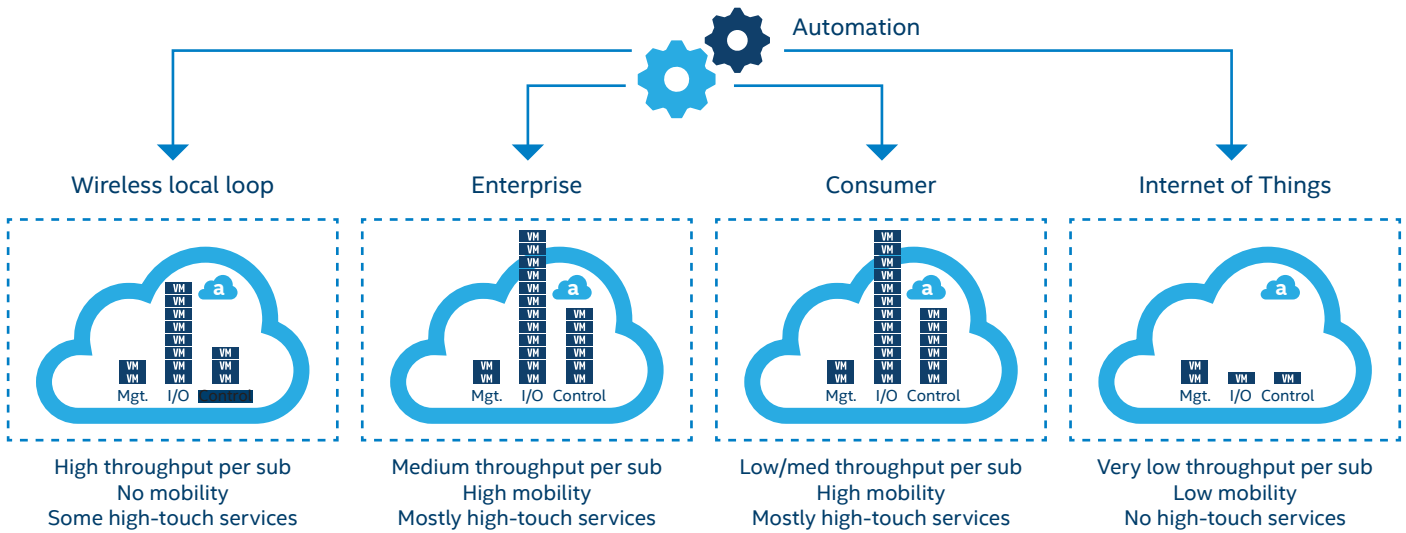
### Affirmed Mobile Core\*

Affirmed Networks' 5G EPC solution enables operators to economically scale networks, deliver differentiated services tailored to specific use cases, take advantage of 5G capabilities today, scale in near-real time to handle more traffic, simplify network operations, and rapidly create and launch new services.

Affirmed Networks has demonstrated leading per-server throughput on its virtualized platforms, and has recognized

and seized the opportunity to leverage the Intel PAC to demonstrate a performance approaching 400 Gbps per server when limitations of the PCI bus are overcome.

By combining the Affirmed Mobile Core with network slicing and service automation, operators can capture new revenue streams and deploy network slices that reduce time to market and operational costs up to 90 percent.<sup>4</sup>



### Enabling a breadth of 5GCN use cases

- **Rapid service creation and delivery:** Deliver customized services with fine-grained network slicing and enable rapid feature development and easy integration with third-party application and content providers using a microservices architecture.
- **Superior customer experience:** Efficiently gather near-real-time network and subscriber intelligence using integrated virtual probes and deliver faster service activation times and self-service capabilities with automated service provisioning.
- **Value-add services:** Quickly, easily chain together service features, accelerate new service creation based on the requirement for DPI, optimize video, offer proxy services, and enhance security, with the virtualized GiLAN and DPI solution.
- **EPC as a Service:** Software-based approach enables rapid delivery of new, innovative mobile services and cost-effective network scalability to support exponential mobile data growth.

## Conclusion

Intel, Dell EMC, and Affirmed Networks have presented 200 Gbps optimized FPGA-accelerated NGCN that enables communications service providers to fully realize the benefits of 5G through COTS hardware.<sup>1</sup> This cost-effective, scalable solution brings flexibility to meet the requirements for high capacity, high throughput, and lower latency deployments, as well as low power and small footprint deployment. This paper demonstrates the performance increases, flexibility, and breadth of NGCN/vEPC by taking advantage of VPP and DPDK optimization, as well as hardware acceleration through Intel FPGA-based PAC and the integration of advanced hardware and software capabilities.

The next generation of Intel FPGA families will allow further acceleration enhancements and throughput gains. PCIe Gen 4 (expected in 2020) and extending the solution to terminate 400 Gbps on a single, dual-socket server will enable new services in 5G.

## Learn more

For more information about Intel FPGAs, visit [intel.com/fpga](https://intel.com/fpga).

Learn more about [Intel FPGA PAC N3000](#).

Find out more about 5G at [intel.com/5G](https://intel.com/5G).

Read an [article on 5G network transformation](#).

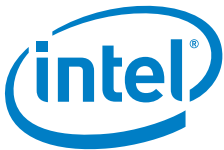
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Find out more about Affirmed Network's solutions for 5G and the communications industry at [affirmednetworks.com](https://affirmednetworks.com).



1. Intel does not control or audit third-party data. You should review this content, consult other sources, and confirm whether referenced data are accurate.

2. [https://www.affirmednetworks.com/wp-content/uploads/2018/06/Affirmed\\_Intel\\_vEPC\\_performance\\_report.pdf](https://www.affirmednetworks.com/wp-content/uploads/2018/06/Affirmed_Intel_vEPC_performance_report.pdf).

3. 17 Dell EMC internal analysis, February 2018, comparing to the Dell EMC PowerEdge M1000e with a legacy MXL switch.

4. <https://cdn2.hubspot.net/hubfs/4933617/Papers/Affirmed%20Race4Rev%20Paper.pdf>.

Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit [intel.com/benchmarks](https://intel.com/benchmarks).

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